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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/687,199 | 10/16/2003 | Lakhbeer S. Sidhu | A1186 | 7140 |

45851 7590 03/08/2005

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| EXAMINER | |
|---|---|
| TRAN, MAI HUONG C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/687,199 | SIDHU ET AL. | |
| | Examiner | Art Unit | |
| | Mai-Huong Tran | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *20 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,16-19,22-24 and 30-36* is/are rejected.

7)☐ Claim(s) *14,15 and 25-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restriction*

Application's election without traverse of Group I (Claims 1-19 and 22-36) drawn to a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 20-21 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

### Drawings

The drawings are objected to for the following reasons.

Formal drawing is required for clarity.

### Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 10-11, 13, 16-19, 22, 30-36 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,624,499 to Kothandaraman et al.

Regarding to claim 1, Kothandaraman discloses a fuse formed on an integrated circuit substrate, comprising a fuse link 106 that is programmed by applying a programming current (col. 3, lines 21-55); and at least one heat sink structure 401 (cols. 3-4, figs. 8A, 8B). The intended use limitation ('wherein when the programming current is being applied, at least part of the at least one heat sink structure carries heat from the fuse link to the integrated circuit substrate without carrying current') does not structurally distinguish the claimed invention over Kothandaraman's reference.

Regarding to claims 2 and 32, the fuse wherein the fuse link comprises polysilicon (col. 5, lines (38-43).

Regarding to claims 3 and 31, the fuse wherein the fuse link comprises crystalline silicon (col. 5, lines (38-43).

Regarding to claim 4, the fuse wherein the fuse link comprises crystalline silicon having a p-n junction (col. 6, lines 54-55).

Regarding to claims 5 and 33, the fuse wherein the fuse link comprises crystalline silicon having a silicide coating and having a p-n junction (cols. 3-6).

Regarding to claim 6, the fuse wherein the fuse link comprises polysilicon covered with a layer of material having a lower resistivity than the polysilicon (col. 6, lines 21-22).

Regarding to claims 7 and 34-35, the fuse wherein the fuse link comprises polysilicon 112; and a layer of silicide 114 on top of the polysilicon (col. 5, lines 58-64).

Regarding to claim 8, the fuse wherein the fuse link comprises a silicided polysilicon link and wherein the at least one heat sink structure comprises a separate heat sink at either end of the fuse link (col. 4, lines 25-38, and fig. 8A).

Regarding to claim 10, the fuse wherein the at least one heat sink structure comprises metal that conveys heat from the fuse to the substrate without conducting current (col. 4, lines 35-38).

Regarding to claims 11 and 23-24, the fuse wherein the at least one heat sink structure comprises at least one metal-filled contact hole that conveys heat from the fuse to the substrate without conducting current (col. 4, lines 25-38).

Regarding to claim 13, the fuse wherein the fuse link comprises polysilicon with a layer of silicide, wherein the layer of silicide has a current-crowding structure that crowds the programming current applied to the fuse link (col. 3, lines 22-67, col. 4, lines 1-2).

Regarding to claim 16, the fuse wherein the fuse link comprises polysilicon having a p-type region and an n-type region that form a p-n junction (col. 6, lines 54-61).

Regarding to claim 17, the fuse wherein the fuse link comprises polysilicon having a p-n junction and a silicide layer having a narrowed portion located at the p-n junction (col. 6, lines 54-61).

Regarding to claim 18, the fuse wherein the at least one heat sink structure helps to blow the fuse at a given position within the fuse link and wherein the fuse link comprises polysilicon having a p-n junction at the given position (col. 6, lines 54-61).

Regarding to claim 19, the fuse wherein the at least one heat sink structure helps to blow the fuse at a given position within the fuse link, wherein the fuse link comprises polysilicon having a p-n junction at the given position, and wherein the fuse further comprises a silicide layer on the polysilicon having a narrowed region that crowds the programming current in the silicide layer during programming (cols. 3-6).

Regarding to claims 22, Kothandaraman et al. disclose a fuse on an integrated circuit substrate comprising a fuse link having a polysilicon line and a layer of silicide on the polysilicon line, wherein the fuse link has first and second ends; and first and second metal lines that apply a programming current to the fuse link that flows from the first end of the fuse link to the second end of the fuse link and programs the fuse link by creating an open circuit in the silicide layer, wherein the polysilicon line comprises a p-type doped region and an n-type doped region that form a p-n junction (cols. 3-6).

Regarding to claim 30, Kothandaraman et al. disclose a fuse on an integrated circuit substrate comprising a fuse link having a semiconductor line and a thin-film conductive layer on the semiconductor line, wherein the fuse link has first and second ends; and first and second metal lines that apply a programming current to the fuse link that flows from the first end of the fuse link to the second end of the fuse link and programs the fuse link by creating an open circuit in the thin-film conductive layer, wherein the semiconductor line comprises a p-type doped region and an n-typed doped region that form a p-n junction (cols. 3-6).

Regarding to claim 36, the fuse wherein the substrate comprises a silicon-on-insulator substrate having a buried oxide layer that is adjacent to the semiconductor line (col. 4, lines 13-67, col. 5, lines 1-22, and fig. 8B).

## Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,624,499 to Kothandaraman et al. in view of the remark.

Regarding to claim 9, Kothandaraman discloses the fuse wherein the fuse link comprises a silicided polysilicon link and wherein the at least one heat sink structure comprises a separate heat sink at either end of the fuse link (col. 4, lines 25-38, and fig. 8A). However, Kothandaraman doesn't disclose a heat sink at a middle position in the fuse link. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a heat sink at a middle position in the fuse link, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

Regarding to claim 12, Kothandaraman discloses the fuse wherein the integrated circuit substrate is covered with a dielectric layer and wherein the at least one heat sink structure comprises first and second metal contacts at either end of the fuse link that convey heat from the fuse link to the integrated circuit substrate. However, Kothandaraman does not disclose the dielectric layer having first and second openings. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric layer having first and second openings, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

## Allowable Subject Matter

Claims 14, 15, 25-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

## Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran

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